Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Original) A method of manufacturing a split gate flash memory device, comprising the steps of:

(a) providing a semiconductor substrate of a conductivity type opposite to that of a first junction region, the semiconductor substrate being provided with a floating gate, a first spacer surrounding the floating gate, the first junction region of a constant conductivity type, which is overlapped with the first spacer and is formed on the substrate, and a first conductive line contacted with the first spacer and formed on the first junction region;

(b) sequentially forming a first dielectric film, a first conductive film, a second dielectric film and a third dielectric film on an overall upper face of the substrate;

(c) planarizing the third dielectric film by a given thickness so as to expose the second dielectric film;

(d) removing the exposed second dielectric film, and eliminating the remaining third dielectric film;

(e) planarizing the first conductive film and the second dielectric film by a given thickness so as to partially expose the first conductive line and the first conductive film;

(f) forming a fourth dielectric film on a portion of the exposed first conductive line and first conductive film;

(g) eliminating the remaining second dielectric film, and exposing the first conductive film provided in a lower part thereof;

(h) etching the first dielectric film and the first conductive film exposed by the removal of the second dielectric film using the fourth dielectric film as an etch mask, and forming a second gate dielectric film and a word line;

(i) forming a second spacer on a sidewall of the word line;

(j) forming a second junction region of a conductivity type the same as that of the first junction region on the substrate, said second junction region being overlapped with the word line and the second spacer;

(k) forming an interlayer dielectric film having a contact hole for exposing the second junction region, on an entire upper face of the substrate; and

(l) forming a second conductive line contacted with the second junction region through the contact hole.

2. (Original) The method of claim 1, wherein in step (c), the third dielectric film is removed by a given thickness through a chemical mechanical polishing (CMP) until the second dielectric film is exposed.

3. (Original) The method of claim 1, wherein in step (e), the second dielectric film and the first conductive film are removed by a constant thickness through an etching process.

4. (Currently Amended) The method of claim 1, wherein said third dielectric film becomes a buffer layer in ~~the~~ a CMP process to improve step coverage of the first conductive film.

5. (Original) The method of claim 1, wherein said third dielectric film is one of an HDP film, a TEOS film, and a USG film.

6. (Currently Amended) The method of claim 1, wherein said second dielectric film is a stopper layer in ~~the~~ a CMP process of step (c), and is the film to protect the first conductive film provided in a lower part thereof [[,]] from ~~the~~ an etching process of step (e).

7. (Original) The method of claim 1, wherein said first junction region is a source junction region.

8. (Original) The method of claim 1, wherein said second junction region is a drain junction region.

9. (Original) The method of claim 1, wherein said first conductive line is a source line made of polysilicon.

10. (Original) The method of claim 1, wherein said second conductive line is a metallic line.

11. (Currently Amended) The method of claim 1, wherein said fourth dielectric film is an oxide film selectively formed through an oxidation in which the second dielectric film is used as ~~the~~ an etching mask in ~~the (f)~~ step (f).

12. (Original) The method of claim 1, wherein said word line has a uniform width and a sidewall of a vertical structure contacted with the second spacer.

13. (Original) A method of manufacturing a split gate flash memory device, comprising the steps of:

(a) providing a semiconductor substrate of a conductivity type opposite to that of a first junction region, said semiconductor substrate being provided with floating gates spaced from each other, first spacers respectively surrounding the floating gates, the first junction region of a constant conductivity type, which is overlapped with the first spacers and is formed on the substrate, and a first conductive line contacted with the first spacer and formed on the first junction region;

(b) sequentially forming a first dielectric film, a first conductive film, a second dielectric film and a third dielectric film on an overall upper face of the substrate;

(c) planarizing the third dielectric film by a given thickness so as to expose the second dielectric film;

(d) removing the exposed second dielectric film, and eliminating the third dielectric film remained;

(e) planarizing the first conductive film and the second dielectric film by a given thickness so as to partially expose the first conductive line and the first conductive film;

(f) forming a fourth dielectric film on a portion of the exposed first conductive line and first conductive film;

(g) eliminating the second dielectric film remained, and exposing the first conductive film provided in a lower part thereof;

(h) etching the first dielectric film and the first conductive film exposed by the removal of the second dielectric film by using the fourth dielectric film as an etch mask, and forming a second gate dielectric film and a word line;

(i) forming a second spacer on a sidewall of the word line;

(j) forming a second junction region of a conductivity type the same as that of the first junction region on the substrate, said second junction region being overlapped with the word line and the second spacer;

(k) forming an interlayer dielectric film having a contact hole for exposing the second junction region on an entire upper face of the substrate; and

(l) forming a second conductive line contacted with the second junction region through the contact hole.

14. (Canceled)